REMARKS

Double Patenting Rejection

Claims 11-14, 16, 17, 19 and 20 were provisionally rejected under the judicially created obviousness-type double patenting as being unpatentable over claims 11-20 of copending U.S. Patent Application Serial No. 11/436,803. Due to the fact that neither this nor the '803 application have allowed claims, Applicant respectfully requests that the double patenting rejection be held in abeyance until all pending claims have been allowed. Upon allowance of the claims, Applicant will submit a terminal disclaimer to overcome the non-statutory double patenting rejection.

Claim Rejections Under 35 U.S.C. § 102

Claims 1-3 and 5-10 were rejected under 35 U.S.C. § 102(b) as being anticipated by Borkenhagen et al. (U.S. Patent No. 5,067,105). Applicant respectfully traverses this rejection.

The Examiner states in the "1st Point of Argument" of the present office action that *Borkenhagen et al.* teaches that "the relationship between the logical addresses and the corresponding physical addresses are maintained in a memory..." Applicant respectfully maintains that this is not the case with *Borkenhagen et al.* Only the physical address is maintained in memory, the logical address is generated later.

The register 4 of *Borkenhagen et al.* stores only the physical address of each logic card. This is evidenced by the paragraph at column 3, lines 42 – 56 that states "The first 3-bit position, logical Card 0, is loaded with the physical address of a memory card found to have no errors." Multiple other places in this paragraph indicate that only physical addresses are stored in the register 4. Note that the reference to "logical" in this sentence, and elsewhere in this paragraph, refers only to the type of card as being a "logical card" and not the logical address of a card as referred to in col. 3, line 58.

More significantly, col. 4, lines 17 – 19 states that "Of particular significance is the fact that the address translation from logical to physical is done in real time by only two levels of logic." This same paragraph further states that "by using the same logic to convert all memory addresses, the requirement for additional hardware is minimized." This entire paragraph, as well

as the preamble to claim 1, indicate that the invention described in *Borkenhagen et al.* is for "automatically configuring the translation of a logical memory address to a physical memory address..." (see preamble to claim 1). There would not be a need for the claimed invention of *Borkenhagen et al.*, for translation of the logical address to the physical address, if both the physical address and logical address of the logical cards were maintained in memory.

The Applicant's presently claimed subject matter comprises a method for managing multiple memory devices by accessing a look-up table that stores a logical address with its corresponding physical address in memory. There is no requirement for a method for translation since both the logical and corresponding physical addresses are stored in memory and only a read operation is required to obtain them. Thus, the present claims are to a completely different method than that disclosed in *Borkenhagen et al.*

Claim Rejections Under 35 U.S.C. § 103

Claims 4, 11-14, 16, 17, 19 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Borkenhagen et al.* in view of *Daberko* (U.S. Patent No. 5,787,445). Applicant respectfully traverses this rejection.

Applicant believes, from the above remarks, that *Borkenhagen et al.* neither teach nor suggest Applicant's presently claimed subject matter. *Daberko* only discloses flash memory and neither teaches nor suggests Applicant's presently claimed subject matter. Even if it were obvious to combine *Borkenhagen et al.* with *Daberko*, the combination still would not anticipate the present invention as claimed in the amended claims since the combination still does not teach or suggest all of the elements of Applicant's claims.

CONCLUSION

In view of the above remarks, Applicant respectfully requests that the Examiner withdraw the Final Rejection in this case. Please charge any further fees deemed necessary or credit any overpayment to Deposit Account No. 501373.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211.

Respectfully submitted,

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